Sipex

SP703/SP704

Low Power Microprocessor Supervisory with Battery Switch-Over

- Precision Voltage Monitor:
  SP703 at 4.65V
  SP704 at 4.40V
- Reset Time Delay - 200ms
- Debounced TTL/CMOS -
  Compatible Manual - Reset Input
- Minimum component count
- 60µA Maximum Operating Supply Current
- 0.6µA Maximum Battery Backup Current
- 0.1µA Maximum Battery Standby Current
- Power Switching
  250mA Output in V_{CC} Mode (0.6Ω)
  25mA Output in Battery Mode (5Ω)
- Voltage Monitor for Power Fail or
  Low Battery Warning
- Available in 8 pin SO and DIP packages
- RESET asserted down to V_{CC} = 1V
- Pin Compatible Upgrades to
  MAX703/MAX704

Now available in Lead Free

DESCRIPTION

The **SP703/704** devices are microprocessor (µP) supervisory circuits that integrate a myriad of components involved in discrete solutions to monitor power-supply and battery-control functions in µP and digital systems. The series will significantly improve system reliability and operational efficiency when compared to discrete solutions. The features of the **SP703/704** devices include a manual reset input, a µP reset and backup-battery switchover, and power-failure warning. The series is ideal for applications in computers, controllers, intelligent instruments and automotive systems. All designs where it is critical to monitor the power supply to the µP and its related digital components will find the series to be an ideal solution.
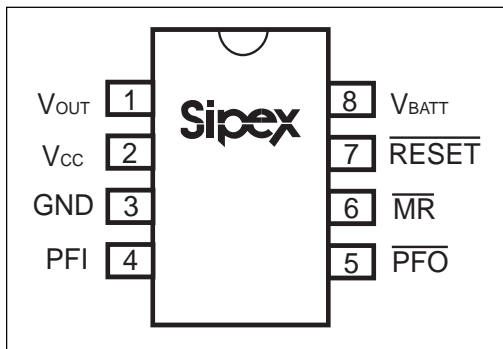
PINOUT
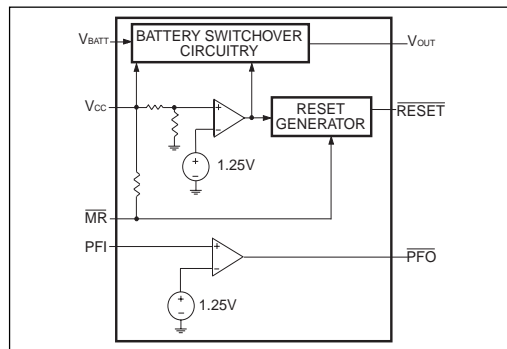
INTERNAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}...-0.3V to 6.0V
V_{BATT}..-0.3V to 6.0V
All Other Inputs.....................................-0.3V to (V_{CC} +0.3V)
Input Current:
    V_{CC}...250mA
    V_{BATT}..50mA
    GND..20mA
Output Current:
    V_{OUT}.....Short-Circuit Protected for up to 10sec
    All Other Inputs.................................20mA

    Rate of Rise, V_{CC},V_{BATT}..................100V/µs
Continuous Power Dissipation.......500mW
    Storage Temperature.......-65°C to +160°C
Lead Temperature(soldering,10sec).................+300°C
ESD Rating.............................4kV Human Body Model

SPECIFICATIONS

V_{cc}=4.75v to 5.50V for SP703, V_{CC} = 4.50V to 5.50V for SP704, V_{BATT}=2.80V, T_A=T_{MIN} to T_{MAX}, typical specified at 25°C, unless otherwise noted.

| PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Operating Voltage Range, V_{CC} or V_{BATT}, NOTE 1	0		5.5	Volts	
Supply Current, I_{SUPPLY},		35	60	µA	excluding I_{OUT}
I_{SUPPLY} in Battery Backup Mode, V_{CC} = 0V, V_{BATT} = 2.8V		0.001	0.6	µA	
V_{BATT} Standby Current, NOTE 2	-0.1		0.02	µA	V_{CC} > V_{BATT} + 0.2V
V_{OUT} Output	V_{CC} - 0.1	V_{CC} - 0.03 V_{CC} - 0.15		Volts	I_{OUT} = 50mA I_{OUT} = 250mA
V_{OUT} in Battery-Backup Mode V_{CC} < V_{BATT} - 0.2V	V_{BATT} -0.15	V_{BATT} - 0.04 V_{BATT} - 0.20		Volts	I_{OUT} = 5mA I_{OUT} = 25mA
Battery Switch Threshold, V_{CC} to V_{BATT}		20 -20		mV	Power-up Power-down
Battery Switchover Hysteresis		40		mV	Peak to Peak
Reset Threshold	4.50 4.25	4.65 4.40	4.75 4.50	Volts	SP703 SP704

SPECIFICATIONS (continued)

V_{cc}=4.75V to 5.50V for SP703, V_{CC} = 4.5 0V to 5.50V for SP704, V_{BATT}=2.80V, T_A=T_{MIN} to T_{MAX}, typical specified at 25°C, unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Reset Threshold Hysteresis		40		mV	Peak to Peak
Reset Pulse Width, t_{RS}	140	200	280	ms	
$\overline{RESET}$ Output Voltage	V_{CC} - 1.5				I_{SOURCE} = 800µA
		0.1	0.4	Volts	I_{SINK} = 3.2mA
		0.004	0.3		I_{SINK} = 50µA, V_{CC} = 1.0V

$\overline{MR}$ Input Threshold
          LOW
          HIGH
	
	2.0
			
			0.8
				
				V	

$\overline{MR}$ Minimum Pulse Width	150			ns	
$\overline{MR}$ to RESET Delay			250	ns	
$\overline{MR}$ Pull Up Current	100	250	600	µA	$\overline{MR}$=0V
PFI Input Threshold	1.200	1.250	1.300	Volts	
PFI Input Current	-25	0.01	25	nA	
$\overline{PFO}$ Output Voltage	V_{CC} - 1.5			Volts	I_{SOURCE} = 800µA
		0.1	0.4		I_{SINK} = 3.2mA

NOTE 1: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2.0V.
NOTE 2: "-" equals the battery-charging current, "+" equals the battery-discharging current.

PINOUT

INTERNAL BLOCK DIAGRAM
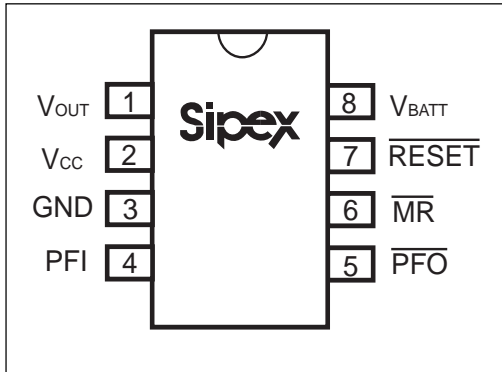
PIN ASSIGNMENTS

Pin 1 —V_{OUT} — Output Supply Voltage. V_{OUT} connects to V_{CC} when V_{CC} is greater than V_{BATT} and V_{CC} is above the reset threshold. When V_{CC} falls below V_{BATT} and V_{CC} is below the reset threshold, V_{OUT} connects to V_{BATT}. Connect a 0.1µF capacitor from V_{OUT} to GND.

Pin 2 — V_{CC} — +5V Supply Input

Pin3 — GND — Ground reference for all signals

Pin 4 — PFI — Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used.

Pin 5 — $\overline{PFO}$ — Power-Fail Output.

Pin 6 — $\overline{MR}$ — Manual Reset Input. This input generates a reset pulse when pulled below 0.8V. This active LOW input is TTL/CMOS compatible and can be shorted to ground with a switch. It has an internal 250µA (typical) pull-up current. Leave this pin floating when not used.
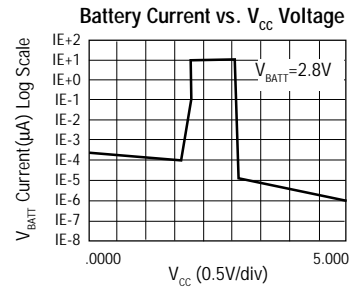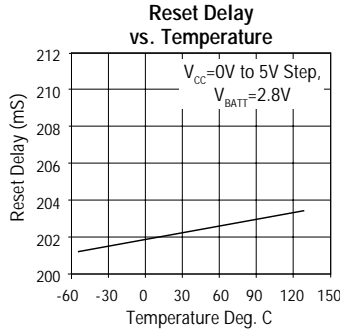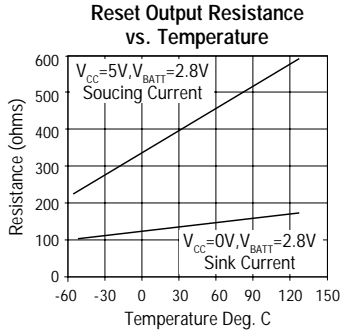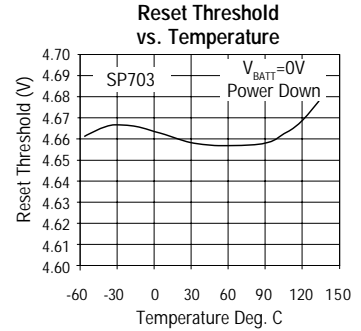
Pin 7 — $\overline{RESET}$ (Active Low)– Reset Output. $\overline{RESET}$ Output goes low whenever V_{CC} falls below the reset threshold or whenever $\overline{MR}$ is pulled below 0.8V for longer than 150nS. $\overline{RESET}$ remains low for 200ms after V_{CC} crosses the reset threshold voltage on power-up or after being triggered by $\overline{MR}$.
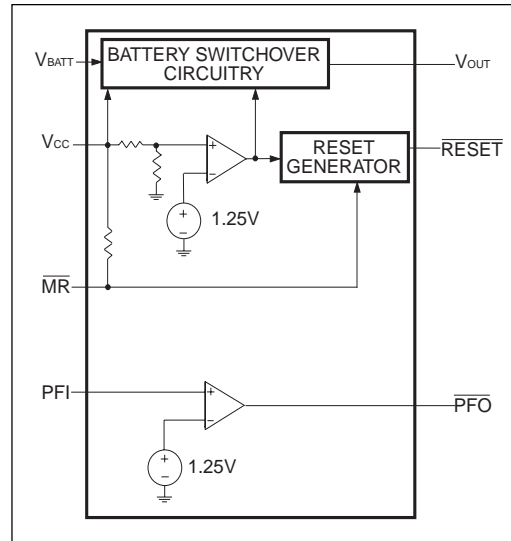
Pin 8 — V_{BATT} — Backup-Battery Input. When V_{CC} falls below the reset threshold, V_{BATT} will be switched to V_{OUT} if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises 20mV above V_{BATT}, V_{OUT} will be reconnected to V_{CC}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.
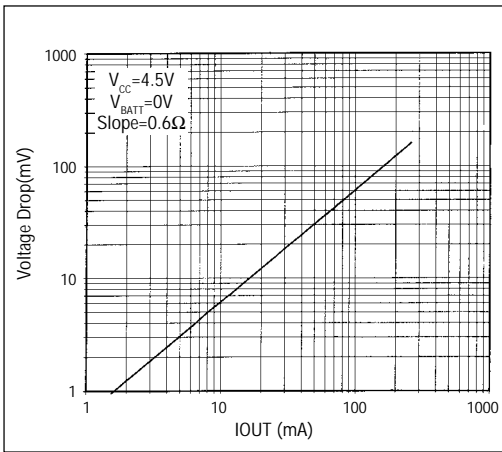
TYPICAL CHARACTERISTICS (25°C, unless otherwise noted)

V_{CC} Supply Current vs. Temperature (Normal Mode)

V_{CC}=5V
V_{BATT}=2.8V

Y-axis: V_{CC} Current (µA) — 19, 23, 27, 31, 35, 39, 43, 47, 51
X-axis: Temperature Deg. C — -60, -30, 0, 30, 60, 90, 120, 150

Battery Supply Current vs. Temperature (Backup Mode)

V_{CC}=0V
V_{BATT}=2.8V

Y-axis: V_{BATT} Current (µA) — -0.1, 0.4, 0.9, 1.4, 1.9, 2.4, 2.9
X-axis: Temperature Deg. C — -60 -40 -20 0 20 40 60 80 100 120 140

PFI Threshold vs. Temperature

V_{CC}=5V
V_{BATT}=0
NO LOAD ON PFO

Y-axis: PFI Threshold (V) — 1.246, 1.248, 1.250, 1.252, 1.254, 1.256
X-axis: Temperature Deg. C — -60, -30, 0, 30, 60, 90, 120, 150

V_{BATT} to V_{OUT} ON Resistance vs. Temperature

V_{CC}=0V
V_{BATT}=2V
V_{BATT}=2.8V
V_{BATT}=4.5V

Y-axis: Resistance (ohms) — 0, 5, 10, 15
X-axis: Temperature Deg. C — -60, -30, 0, 30, 60, 90, 120, 150

V_{CC} to V_{OUT} On Resistance vs. Temperature

V_{CC}=5V
V_{BATT}=0V

Y-axis: Resistance (ohms) — 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9
X-axis: Temperature Deg. C — -60, -30, 0, 30, 60, 90, 120, 150

Reset Threshold vs. Temperature

SP703
V_{BATT}=0V
Power Down

Y-axis: Reset Threshold (V) — 4.60, 4.61, 4.62, 4.63, 4.64, 4.65, 4.66, 4.67, 4.68, 4.69, 4.70
X-axis: Temperature Deg. C — -60, -30, 0, 30, 60, 90, 120, 150

Reset Output Resistance vs. Temperature

V_{CC}=5V,V_{BATT}=2.8V
Soucing Current
V_{CC}=0V,V_{BATT}=2.8V
Sink Current

Y-axis: Resistance (ohms) — 0, 100, 200, 300, 400, 500, 600
X-axis: Temperature Deg. C — -60, -30, 0, 30, 60, 90, 120, 150

Reset Delay vs. Temperature

V_{CC}=0V to 5V Step,
V_{BATT}=2.8V

Y-axis: Reset Delay (mS) — 200, 202, 204, 206, 208, 210, 212
X-axis: Temperature Deg. C — -60, -30, 0, 30, 60, 90, 120, 150

Battery Current vs. V_{CC} Voltage

V_{BATT}=2.8V

Y-axis: V_{BATT} Current (µA) Log Scale — IE-8, IE-7, IE-6, IE-5, IE-4, IE-3, IE-2, IE-1, IE+0, IE+1, IE+2
X-axis: V_{CC} (0.5V/div) — .0000, 5.000

Figure 1. V_{CC} *to* V_{OUT} *Vs. Output Current*
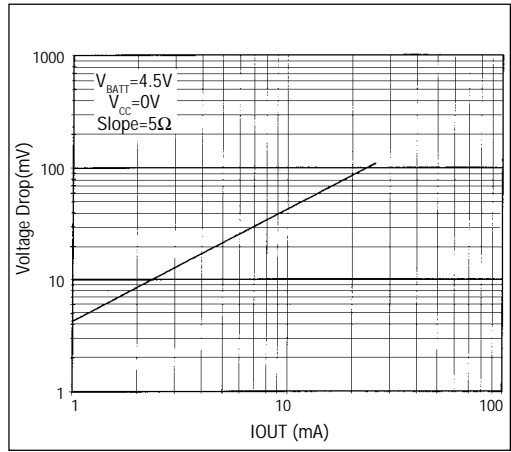

Figure 2. V_{BATT} *to* V_{OUT} *Vs. Output Current*
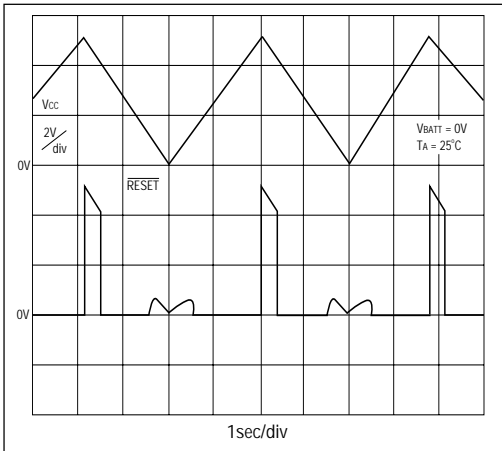

Figure 3A. *SP703* $\overline{RESET}$ *Output Voltage vs. Supply Voltage*
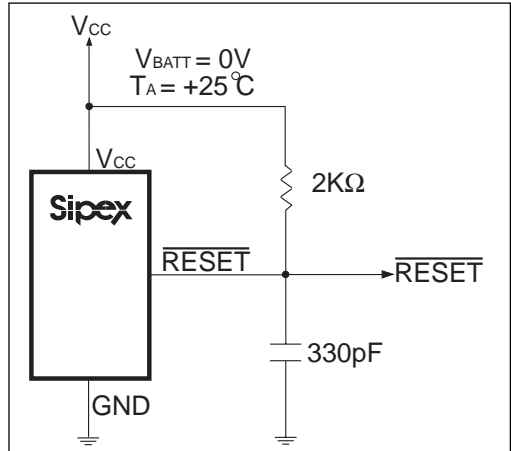

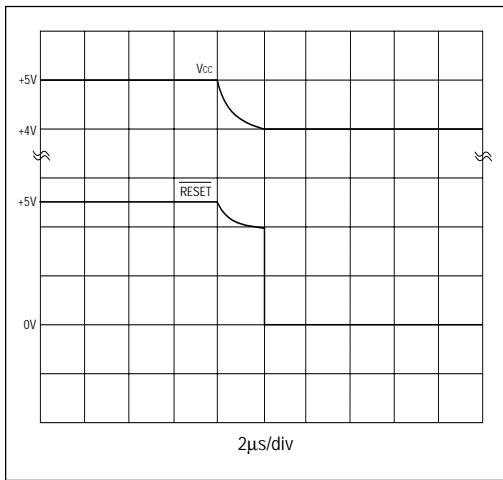**Figure 3B.** *Circuit for the* $\overline{RESET}$ *Output Voltage vs. Supply Voltage*
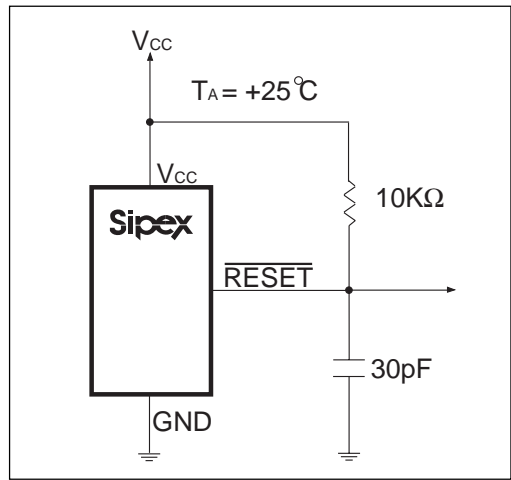
Figure 4A. SP703 $\overline{RESET}$ Response Time

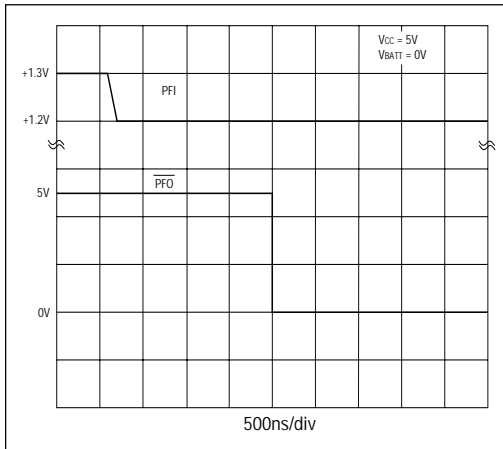*Figure 4B. Circuit for the $\overline{RESET}$ Response Time*

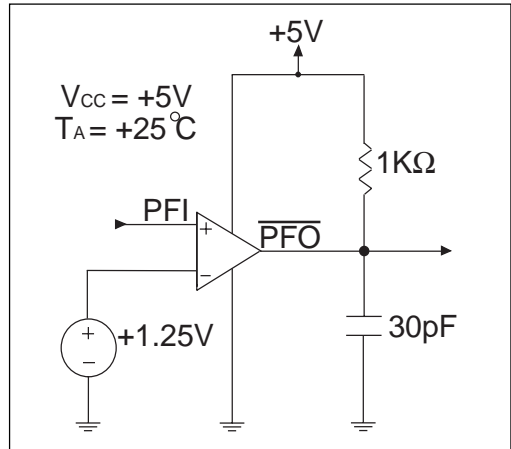*Figure 5A. Power-Fail Comparator Response Time (FALL)*

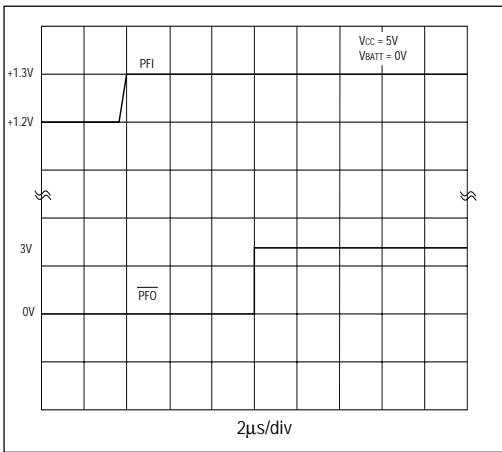*Figure 5B. Circuit for the Power-Fail Comparator Response Time (FALL)*
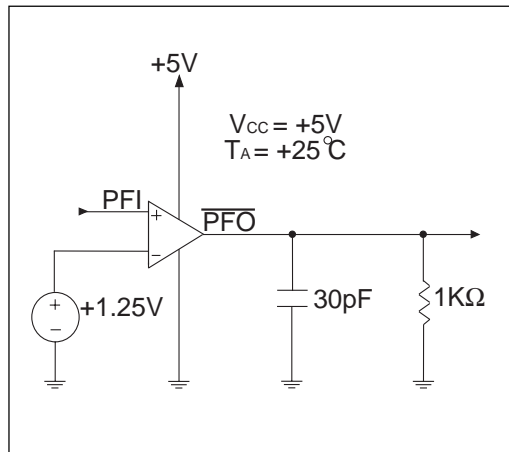
Figure 6A. Power-Fail Comparator Response Time (RISE)

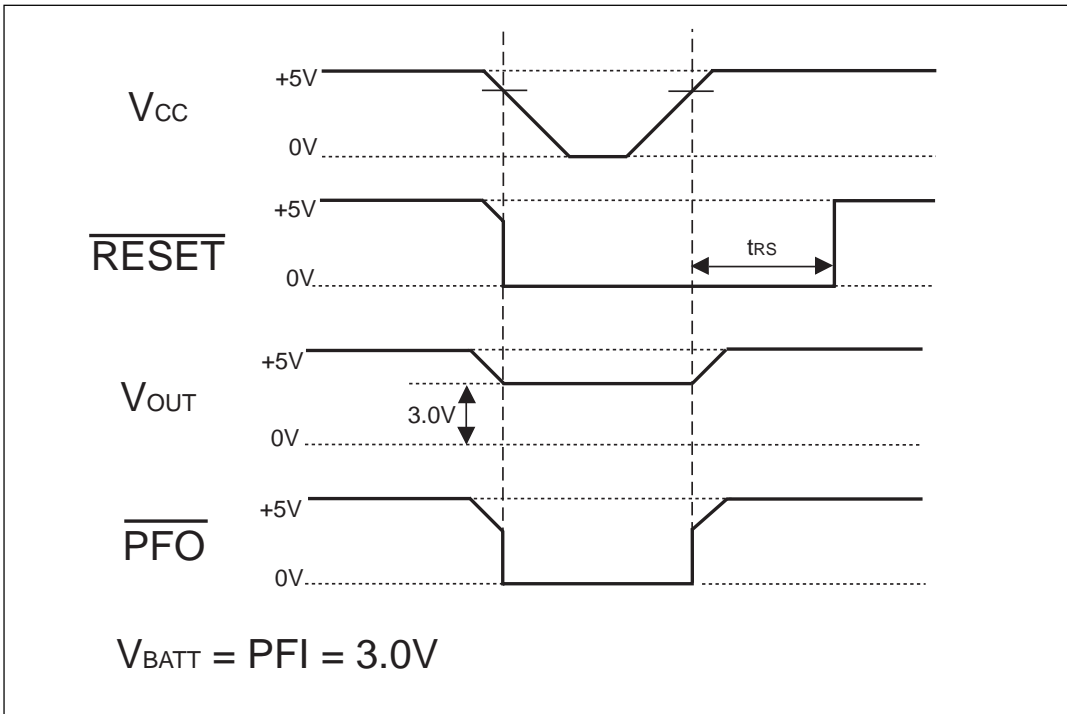*Figure 6B. Circuit for the Power-Fail Comparator Response Time (RISE)*

Figure 7. Timing Diagram

FEATURES

The **SP703/704** devices provide four key functions:

1. A battery backup switching for CMOS RAM, CMOS microprocessors, or other logic.
2. A reset output during power-up, power-down and brownout conditions.
3. A reset pulse if the manual reset has been pulled below 0.8V for at least 150ns.
4. A 1.25V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than +5V.

The **SP703/704** devices differ only in their supply voltage monitor level. The **SP703** generates a reset when V_{CC} drops below 4.65V while the **SP704** generates a reset below 4.4V.

The **SP703/704** devices are ideally suited for applications in automotive systems, intelligent instruments, and battery-powered computers and controllers. All designs into an environment where it is critical to monitor the power supply to the µP and its related digital components will find the **SP703/704** ideal.

THEORY OF OPERATION

Reset Output

The microprocessor's (µP's) reset input starts the µP in a known state. When the µP is in an unknown state, it should be held in reset. The **SP703/704** assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{\text{RESET}}$ is guaranteed to be a logic low. As V_{CC} rises, $\overline{\text{RESET}}$ remains low. When V_{CC} exceeds the reset threshold, $\overline{\text{RESET}}$ will remain low for 200ms, *Figure 9*. If a brownout condition occurs and V_{CC} dips below the reset threshold, $\overline{\text{RESET}}$ is triggered. Each time $\overline{\text{RESET}}$ is triggered, it stays low for the reset pulse width interval. If a brownout condition interrupts a previously initiated reset pulse, the reset pulse continues for another 200ms. On power-down, once V_{CC} goes below the threshold, $\overline{\text{RESET}}$ is guaranteed to be logic low until V_{CC} drops below 1V. $\overline{\text{RESET}}$ is also triggered by a manual reset
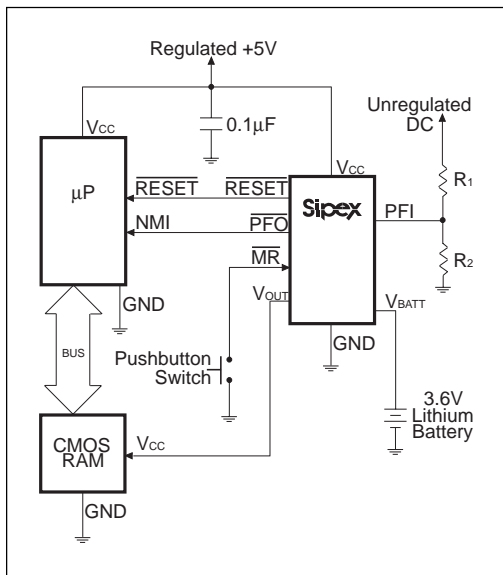

Figure 8. Typical Operating Circuit

Power-Fail Comparator

The Power-Fail Comparator can be used as an under-voltage detector to signal the failing of a power supply (it is completely separate from the rest of the circuitry and does not need to be dedicated to this function). The PFI input is compared to an internal 1.25V reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The external voltage divider drives PFI to sense the unregulated DC input to the +5V regulator. The voltage-divider ratio can be chosen such that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. $\overline{PFO}$ then triggers an interrupt which signals the μP to prepare for power-down.

When V_{BATT} connects to V_{OUT}, the power-fail comparator is turned off and $\overline{PFO}$ is forced low to conserve backup-battery power.

CONDITION	SW1	SW2
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold and V_{CC} < V_{BATT}	Closed	Open

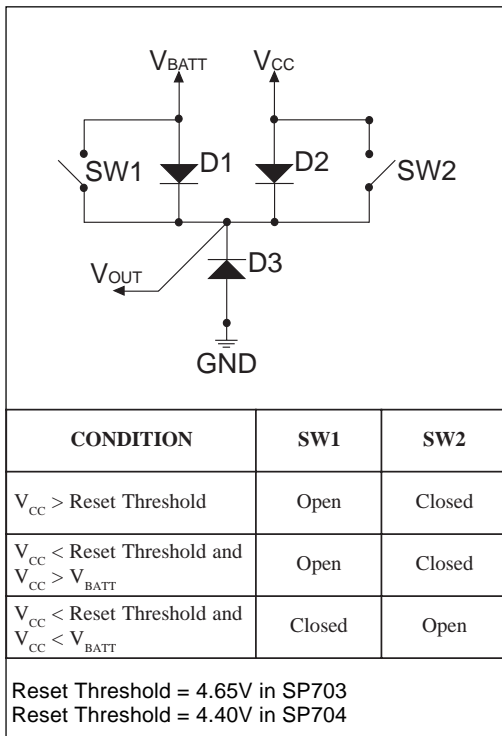Reset Threshold = 4.65V in SP703
Reset Threshold = 4.40V in SP704

Figure 9. BACKUP-BATTERY Switchover Block Diagram

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at V_{BATT}, the RAM is assured to have power if V_{CC} fails. As long as V_{CC} exceeds the reset threshold, V_{OUT} connects to V_{CC} through a 0.6Ω PMOS power switch. Once V_{CC} falls below the reset threshold, V_{CC} or V_{BATT}, whichever is higher, switches to V_{OUT}. V_{BATT} connects to V_{OUT} through a 5Ω switch only when V_{CC} is below the reset threshold and V_{BATT} is greater than V_{CC}.

When V_{CC} exceeds the reset threshold, it is connected to V_{OUT}, regardless of the voltage applied to V_{BATT} *Figure 9*. During this time, the diode (D1) between V_{BATT} and V_{OUT} will conduct current from V_{BATT} to V_{OUT} if V_{BATT} is more than .6V above V_{OUT}.

When V_{BATT} connects to V_{OUT}, backup mode is activated and the internal circuitry will be powered from the battery *Figure 10*. When V_{CC} is just below V_{BATT}, in the backup mode the current drawn from V_{BATT} will be typically 30μA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 0.6μA.

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}
V_{OUT}	Connected to V_{BATT} through an internal 8Ω PMOS switch
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than $0.6\mu A$, as long as $V_{CC} < V_{BATT}$ - 1V.
PFI	Power-fail comparator is disabled.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
$\overline{MR}$	Manual Reset is disabled

Figure 10. Input and Output Status in Battery-Backup Mode. To enter the Battery-Backup mode, V_{CC} must be less than the Reset threshold and less than V_{BATT}

Using a High Capacity Capacitor as a Backup Power Source

VBATT has the same operating voltage range as VCC, and the battery-switchover threshold voltages are typically +20mV centered at VBATT, allowing use of a capacitor and a simple charging circuit as a backup source (see *Figure 12*).

PART NUMBER	MAXIMUM BACKUP-BATTERY VOLTAGE [V]
SP703	4.80
SP704	4.55

Figure 11. Allowable BACKUP-BATTERY Voltages

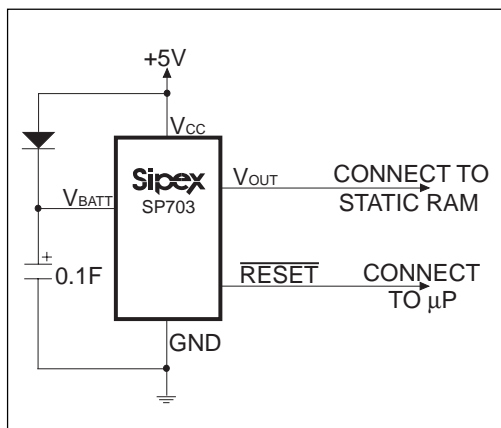*Figure 12. Backup Power Source Using High Capacity Capacitor with SP703 and a +5V ±5% Supply*

If VCC is above the reset threshold and VBATT is 0.5V above VCC, current flows to V_{OUT} and VCC from VBATT until the voltage at VBATT is less than 0.5V above VCC.

Leakage current through the capacitor charging diode and the **SP703/704** internal power diode eventually discharges the capacitor to VCC. Also, if VCC and VBATT start from 0.5V above the reset threshold and power is lost at VCC, the capacitor on VBATT discharges through VCC until VBATT reaches the reset threshold; the **SP703/704** then switches to battery-backup mode.
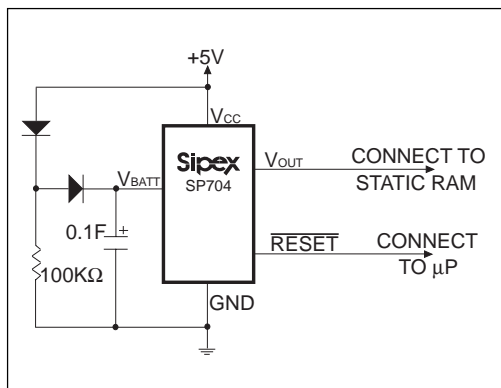

Figure 13. Backup Power Source Using High Capacity Capacitor with SP704 and a +5V ±10% Supply

$$V_{TRIP} = \frac{1.25}{\left(\dfrac{R_2}{R_1 + R_2}\right)}$$

$$\frac{1.25}{R_2} = \frac{V_L - 1.25}{R_1} + \frac{5.0 - 1.25}{R_3}$$

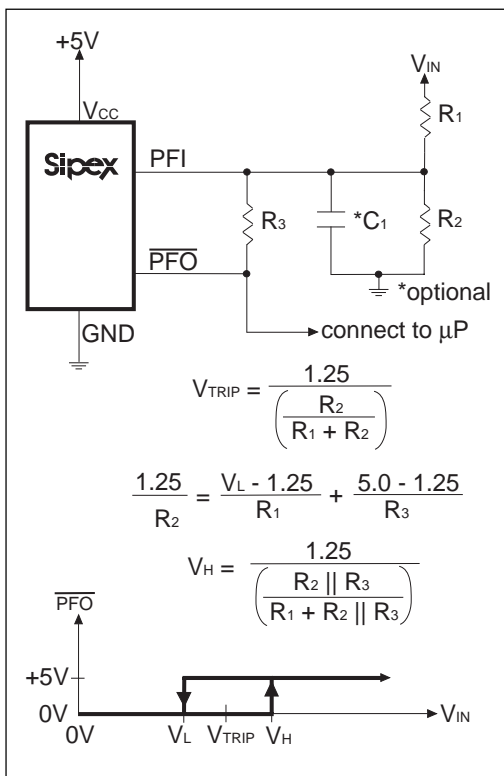$$V_H = \frac{1.25}{\left(\dfrac{R_2 \| R_3}{R_1 + R_2 \| R_3}\right)}$$

Figure 14. Adding Hysteresis to the POWER-FAIL Comparator

Allowable Backup Power-Source Batteries

Lithium batteries work very well as backup batteries due to very low self-discharge rate and high energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal. Any battery with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be connected directly to the V_{BATT} input of this series with no additional circuitry; see *Figure 8*. However, batteries with open-circuit voltages that are greater than this value cannot be used for backup, as current is sourced into V_{OUT} through the diode *(D1 in Figure 9)* when V_{CC} is close to the reset threshold.

Operation Without a Backup Power Source

If a backup power source is not used, ground V_{BATT} and connect V_{OUT} to V_{CC}. Since there is no need to switch over to any backup power source, V_{OUT} does not need to be switched. A direct connection to V_{CC} eliminates any voltage drops across the switch which may push V_{OUT} below V_{CC}.

Replacing the Backup Battery

The backup battery can be removed while V_{CC} remains valid, without danger of triggering RESET/$\overline{RESET}$. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when V_{IN} is close to its trip point. *Figure 14* shows how to add hysteresis to the power-fail comparator. Select the ratio of R_1 and R_2 such that PFI sees 1.25V when V_{IN} falls to its trip point (V_{TRIP}). R_3 adds the hysteresis. It will typically be an order of magnitude greater (about 10 times) than R_1 or R_2. The current through R_1 and R_2 should be at least 1μA to ensure that the 25nA (max) PFI input current does not shift the trip point. R_3 should be larger than 10KΩ so it does not load down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply rail using the circuit of *Figure 15*. When the negative rail is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and the resistors, R1 and R2.
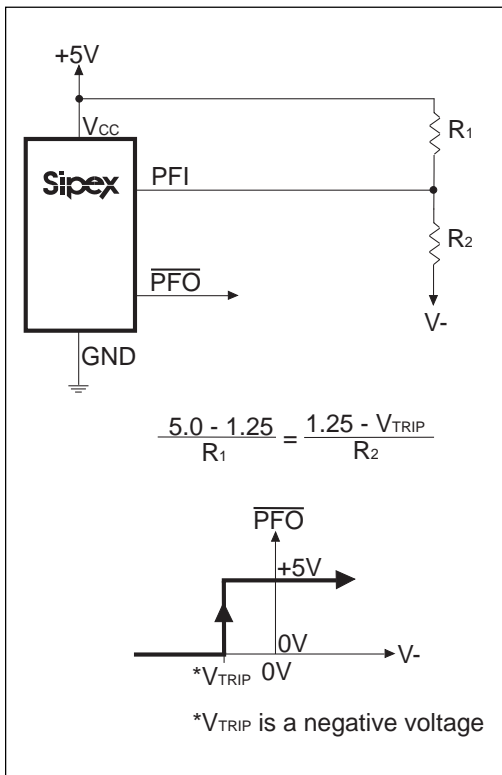
$$\frac{5.0 - 1.25}{R_1} = \frac{1.25 - V_{TRIP}}{R_2}$$

*V_{TRIP} is a negative voltage

Figure 15. Monitoring a Negative Voltage

Figure 16. Interfacing to Microprocessors with Bidirectional $\overline{RESET}$ I/O

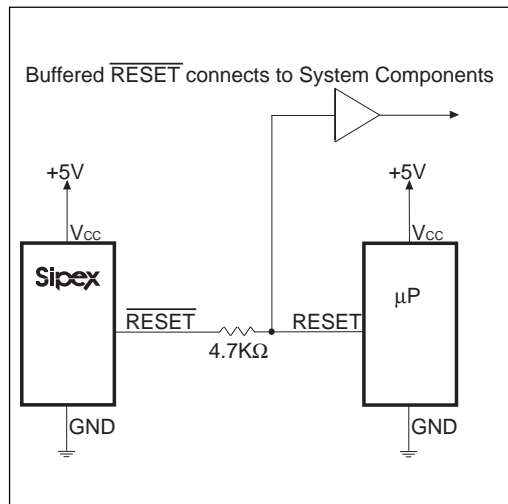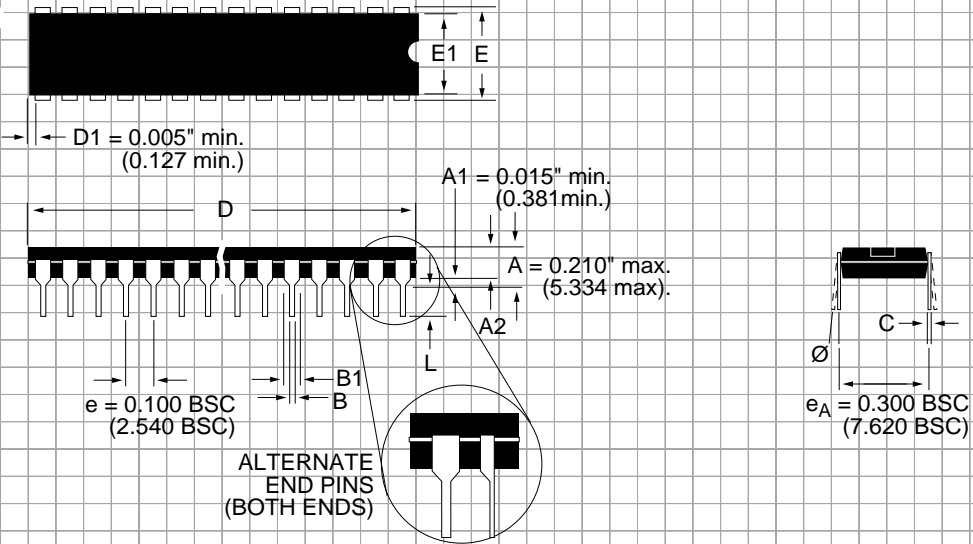## Interfacing to Microprocessors with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with this series' $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the μP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor between the $\overline{RESET}$ output and the μP reset I/O, as in *Figure 16*. Buffer the $\overline{RESET}$ output to other system components.

PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

E1 E

D1 = 0.005" min.
(0.127 min.)

A1 = 0.015" min.
(0.381 min.)

A = 0.210" max.
(5.334 max).

A2

L

D

e = 0.100 BSC
(2.540 BSC)

B1
B

ALTERNATE
END PINS
(BOTH ENDS)

C

Ø

e$_A$ = 0.300 BSC
(7.620 BSC)

DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)
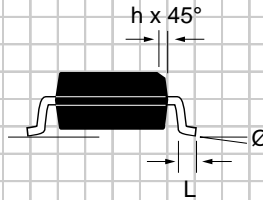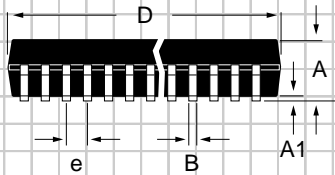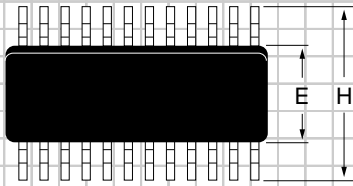
DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249
B	0.014/0.019 (0.35/0.49)
D	0.189/0.197 (4.80/5.00)
E	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP703CN	0°C to +70°C	8-Pin NSOIC
SP703CP	0°C to +70°C	8-Pin PDIP
SP703EN	-40°C to +85°C	8-Pin NSOIC
SP703EP	-40°C to +85°C	8-Pin PDIP
SP704CN	0°C to +70°C	8-Pin NSOIC
SP704CP	0°C to +70°C	8-Pin PDIP
SP704EN	-40°C to +85°C	8-Pin NSOIC
SP704EP	-40°C to +85°C	8-Pin PDIP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Available in lead free packaging. To order, add "-L" suffix to the part number.
Example: SP6660EU/TR=Tape & Reel. SP6660EU-L/TR = lead free.

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